New Fault Tolerant Design Methodology Applied to Middleware Switch Processor

Vladimir Petrovic, Marko Ilic, Gunter Schoof and Zoran Stamenkovic

Abstract - In this paper is presented a new fault tolerant design methodology which provides protection against three most important radiation effects – single event transients (SET), single event upsets (SEU) and single event latchup (SEL). SETs and SEUs are mitigated using the hardware redundancy. Protection against SEL effects is provided by specially designed SEL power protection cell. Combination of different protection techniques is the basis for new fault tolerant design methodology. Middleware Switch processor, which is the main part of Spacecraft Area Network is implemented using the presented design methodology and implementation characteristics are discussed.

Keywords – fault tolerant design, ASIC, single event effects, radiation effects, redundancy, design methodology.

I. Introduction

The main requirement of the space and safety-critical systems is high reliability. In the environments where is hard or even impossible to provide maintenance (space and military applications), it is very important to deploy the circuits and systems which can tolerate faults. Practically, almost all SEU and SET fault-tolerant techniques are based on the redundancy. Few most used types of the redundancy are listed below:

- Hardware redundancy
- Information redundancy
- Time redundancy
- Software redundancy.

In this paper, only the hardware redundancy will be discussed. As the technology allows for smaller transistors, the digital cells get smaller and, therefore, the hardware redundancy becomes more popular. The hardware redundancy provides masking of faults and protects the circuit (or system) from failure. Common hardware-redundancy techniques are the triple modular redundancy (TMR) and the double modular redundancy (DMR).

The triple modular redundancy was mentioned for the first time in the literature in 1956 by J. Von Neumann [1]. The redundant circuit consists of three identical modules and a 3-input majority voter (Fig. 1.a). The voter's function is to pass through the major input value to the output. As we speak about digital circuits, the modules are memory elements such as flip-flops or latches. The main disadvantage of this technique is that the system fails in case of a faulty voter. Therefore, a new triple voting logic was developed to complete the circuit redundancy (Fig. 1.b). Each of the three voters is fed from outputs of all three memory modules. This technique is known in the literature as the full triple modular redundancy. A detailed analysis of the triple modular redundancy is presented in [2].

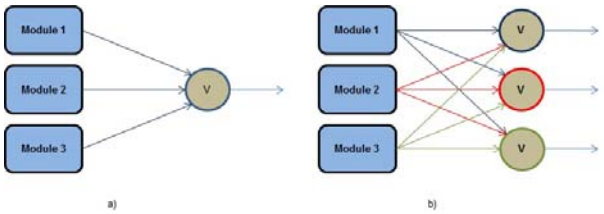

Fig. 1. Triple modular redundancy:
a) single voting, b) full voting

In order to reduce the high hardware overhead produced by the TMR [3], [4] and keep the design reliability high, implementation can be performed using the double modular redundancy with self-voting [5]. A DMR circuit can be designed in two versions: single-voter version and double-voter version. Both versions are shown in Fig. 2. In the literature is possible to find a "C element" as self-voting structure.

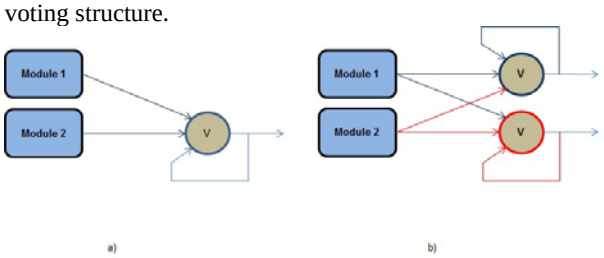

Fig. 2. Dual modular redundancy:
a) single voting, b) full voting

Regarding latchup effects (SEL – single event latchup), all the known techniques for latchup mitigation are classified in three main groups, which are discussed below.

First group uses the current sensors at the board level to detect the excessive current induced by the latchup. The power supply of the affected device is switched-off and, after a pre-specified (long enough) period of time, reestablished again. This approach suffers from a serious drawback: the circuit state is destroyed and cannot be recovered. In addition, the board protection circuits must be designed with special care and the following requirements have to be met:

- Proper decoupling of ICs,

Vladimir Petrovic, Marko Ilic, Gunter Schoof and Zoran Stamenkovic are with the Innovations for High Performance, IHP GmbH, Im Technologiepark 25, 15236 Frankfurt Oder, Germany, E-mail: {petrovic, schoof, stamenkovic}@ihp-microelectronics.com; markoilic2211@gmail.com

- Clamping of outputs with diodes when driving inductive loads,
- Clamping of inputs with diodes if the input signal exceeds the power supply voltage,
- Use of star grounds in high-current applications.

Second latchup effect mitigation approach [6] is based on introduction of an epitaxial-buried layer process and reduction of the well resistivity. However, this modification incurs additional costs and may impact circuit performance (the breakdown voltage, for example).

Third latchup effect mitigation approach [7] uses guard rings (additional N-type and P-type regions) that break the parasitic bipolar transistor structure. This solution is very efficient but can result in excessive circuit area and, therefore, price.

In order to have an automated design flow for the fault-tolerant circuits, it is essential to design the specific components which are not present in standard or radiation hardened design kits. Each component, described in this paper, provides a protection related to the particular effect. A circuit for the latchup protection is described first. Details of the redundant circuits with separated power domains are presented in the following section. Fault tolerant technique is applied on the Spacecraft Area Network (SCAN) main processor, which is in literature known as Middleware Switch processor [8][9].

II. Integrated Latchup Protection

Based on the Latchup Protection Technology (LPT) [10] is developed a circuit which can be integrated in an ASIC as power control cell. The idea is to control the current flow of smaller standard cell areas with integrated latchup protection circuits, instead of the nowadays external LPT based protection circuits. The most interesting advantage is a combination of the redundant circuits, used for protection against upsets and transients, and High-Current-Flow protection circuits, used for protection against potential destructive latchup effects. Redundancy provides stable circuit states during latchup protection phase [11]. With LPT technology this was not the case. Therefore, the paper presents the approach which provides the protection against upsets, transients and latchup effects without expensive technology changes.

Block-diagram of SPS cell is represented in Fig. 3. It consists of current-flow sensor/driver, feed-back block, control block and communication interface for the SPS power network controller (PNC).

The most important component in the SPS circuit is a current sensor. It is in the same time a current driver, used to provide the power supply for the logic which needs to be protected against latchup effect. It is basically a PMOS transistor with wide channel, used in the linear (ohmic) region. The feed-back logic, represented in Fig. 3, provides important information about the current-flow status in the controlled circuit (standard cells). In case that sensor (CSD) detects a higher current than usual it will automatically provide related signal and the feed-back circuit together with the control logic turns-off the power supply of controlled standard cells, where the latchup or high-current flow occurred. The control-logic block communicates with the power network. The SPS cell informs a power network about the current status of the protection mode – whether a protection is activated due to latchup effect. On the other hand, if protection mode was triggered, a power network provides information to the SPS cell when protection mode should be deactivated.

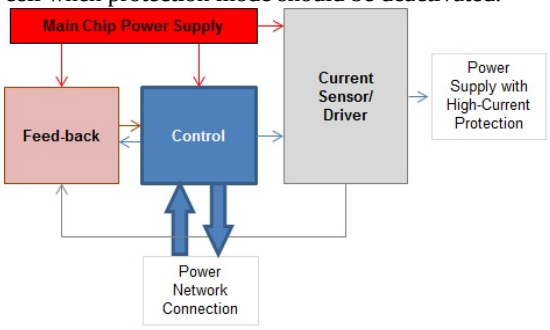

Fig. 3. Block diagram of SPS cell

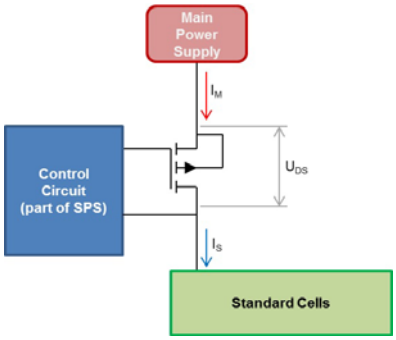

Fig. 4. Block diagram of current sensor/driver transistor

At this point is important to explain how a PMOS transistor provides enough power to standard cells during operation in the ohmic region and to notice a difference between quality of standard power supply and PMOS based power supply. Following the output characteristics of PMOS transistor for constant voltage between gate and source (2.5V), it is possible to notice that linear region goes up to 0.9V of drain-source voltage and 1mA drain current. If standard cells (represented as green block in Fig. 4) require more power, the goal should be providing more current with lower U_{DS} voltage. It is clear that in this case the required scenario is not possible, because the increase of the current increases the U_{DS} voltage, what directly provides lower voltage for the standard cell power supply. Therefore, the only way is to find a trade-off between required current intensity for the supplied circuit (standard cells) and the voltage of the sensor/driver transistor.

The maximal current provided by the sensor/driver transistor of 5µm channel width is between 250µA and 750µA. The maximal voltage drop is about 0.6V for

operational mode when the transistor is used as a driver. Therefore, the power provided by this transistor is not more than 450μW, what is enough to supply 2 flip-flops and few combinational cells.

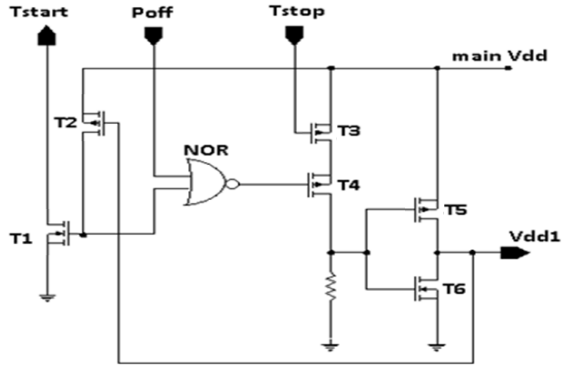

Fig. 5. Simplified SPS Schematic

In Fig. 5 is presented the simplified SPS schematic. In case that output pin Vdd1 is short-circuited, the transistor T5 (sensor/driver transistor) conducts more current than usual and the voltage between source and drain is higher. That means - the voltage on drain of the PMOS (T5) transistor is being lowered. The feedback line from the Vdd1 pin causes transistor T2 to activate when mentioned voltage is under the threshold voltage. Automatically, the transistor T1 will trigger Tstart (low active) output pin.

In order to wake up the power switch circuit (SPS) from the latchup protection mode, it is required to provide an impulse on the "Tstop" pin. This impulse should stop the current flow through the transistor T3 and set the gates of transistors T5 and T6 on the low voltage level. The transistor T5 should activate and provide power supply on Vdd1 output pin. The feedback line is deactivating the transistors T2 and T1, where "Tstart" pin should be set on the high voltage level, whereby latchup protection sequence is finished.

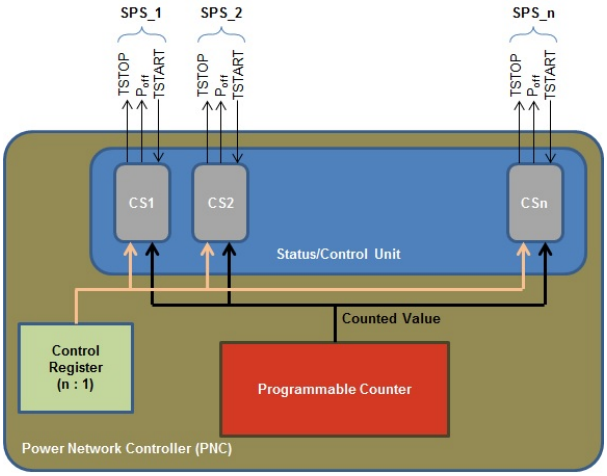

Fig. 6. Power Network Controller (PNC) block diagram

Very important block for correct SPS operation is power network controller (PNC). PNC is a digital subsystem which controls all latchup protection circuits (SPS cells) in the fault-tolerant digital system. It is designed to communicate with all SPS cells independently. It consists of programmable counter and control circuits.

Programmable counter defines duration of the latchup protection phase and control circuits are used to provide communication interface with SPS cells. The power network controller complexity is directly related to the redundancy type – DMR or TMR. Block diagram of PNC is shown in Fig. 6.

III. Automated SPS Placement

A very important design automation step is related to the placement of SPS cells. Parallel to the placement of SPS cells should be provided the integration process of the power network controller (PNC) within the standard design steps. Approach for automated SPS cell placement, which is used in the presented work is based on the Cadence Low-Power Implementation flow [12].

Example of a standard ASIC layout view with implemented power supply terminals is represented in Fig. 7. Power rings are not shown in the mentioned figure because they are not relevant for the SPS cell placement.

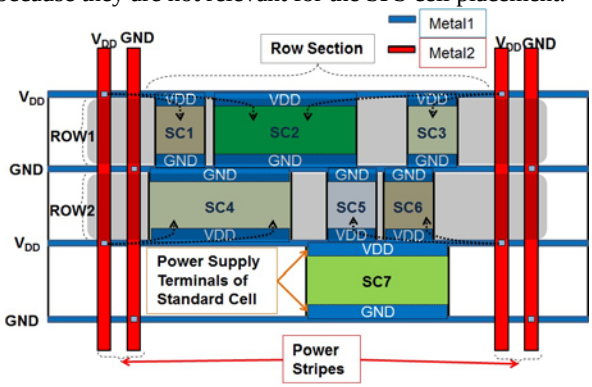

Fig. 7. Standard power network of an ASIC chip

In order to provide basis for the SPS based power network, it is required to provide some information related to the "row section" power consumption of standard power network. The start point for the row power estimation is the power consumption of one "row section". The "row section" is group of standard cells, placed in one row between two power stripes. In Fig. 7 it is possible to notice ROW1 and ROW2 sections. Using the IHP 250nm technology it is estimated that one row section consumes around 400μA. This value is optimal for the SPS cell described before.

ASIC example which integrates SPS cells and redundancy (in this example DMR) is represented in Fig. 8. SEL power switch cells are placed exactly under the power stripes-row crossover points, instead of "filler" cells as usual. The power stripes and power rows at the points

where a SPS is placed are connected only through the SPS cell. A SPS has one output – the controlled power supply line, used for one of the redundant circuits. This requirement is based on the concept of having separate power supplies for the two netlists used for the DMR.

Power supply distribution is provided separately for redundant components. In Fig. 8 is shown that row supply is "broken" in the neighbor SPS cell. SPS cell **1a** and SPS cell **2a** are electrically independent but because of the design rules it is important that wires are not floating. Therefore, row power supply provided by SPS cell **1a** is broken "internally" in SPS cell **2a**. The same approach is used for the redundant power supply, provided by SPS cell **1b** and SPS cell **2b**.

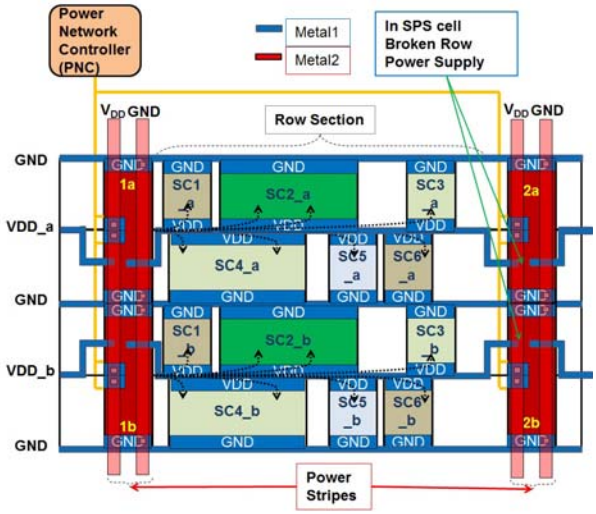

Fig. 8. DMR based circuit with integrated SPS cells

Comparing the standard power network with SPS based power network, it is not hard to notice the most important difference – one SPS cell provides power supplies for all redundancy levels and it is localized in four "row sections". As it was mentioned before, the approach used for the implementation is based on the DMR. For example, if latchup effect occurs in the standard cell "SC5_a", the SPS cell **1a** detects a higher current intensity than usual and switches off the complete "row section" pair. In the same time, the SPS cell **1a** informs the PNC that latchup has been detected. A digital system which includes just latchup protection technique cannot provide correct functionality during the latchup protection phase. Therefore, it is necessary to use the specially designed redundant circuits which support the latchup protection [11].

IV. Case Study: Middleware Switch

During designing a new satellite system, it is usual to face with very complex problems. It is possible to divide them in groups and based on this to find the most optimal solution. The first problem is the long development time of an avionics system. Parallel with it are present the huge costs because of long time required for defining the new interface specifications. The development of very expensive board computers represents the second very important problem. All devices in a satellite communicate with each other through the board computer. Therefore, for every new satellite (or space related) system it is required to define a new device configuration and redesign the board computer. The way for solving these problems was the implementation of a SCAN network, [8] [9]. The central part of the whole SCAN system is the MW switch processor.

In this section are provided the most important information related to the implementation characteristics of the fault-tolerant middleware switch processor. Beside information about power consumption and area of the fault-tolerant processor version, here are represented implementation characteristics of non-fault-tolerant design too. This is done in order to compare two same architectures, which are implemented using two different design approaches. The comparison result provides information related to effects on the implementation characteristics, which a fault-tolerant design has. It is important to notice that test case is realized using reduced version of middleware switch processor.

In the fault-tolerant MW switch version, complete hardware is doubled and for memory protection against potential SEUs is used EDAC and against latchup effect is used the same SPS approach as for the standard cells. As the memory requires more power, few SPS cells are connected in parallel mode. Power network controller is in this example implemented in the SGB25RH process without latchup protection [13]. It is possible to provide two parallel power network controllers with integrated latchup protection but this is not the goal of this discussion.

In order to provide better view on the standard cell type used during implementation, in Table I is presented occupied area in relation to the combinational or sequential cells. It is important to notice that non-combinational cells involving memory blocks and flip-flops. Test case is implemented without latch cells.

After netlist parsing and timing analysis of new DMR-based netlist it is possible to notice increase of power consumption and required silicon area. The implementation results of DMR netlist together with power network controller are presented in Table II.

TABLE I
AREA REGARDING CELL TYPE USING STANDARD DESGIN APPROACH

Standard cell type		Required area [mm²]
Combinational Cells		4.116
Non-combinational Cells	Cache Memory – data + instruction	0.813 3.165
	S3P FIFO	11.626
	Sequential Cells	5.012
TOTAL		24.876

TABLE II
AREA REGARDING CELL TYPE USING FT DESGIN APPROACH

Standard cell type		Required area [mm²]
Combinational Cells		8.232
Non-combinational Cells	Cache Memory – data + instruction	1.626 6.330
	S3P FIFO	23.525
	Sequential Cells	39.903
TOTAL		79.616

The main reason for the area and power overhead is the power network controller. SPS cells doesn't involve any area overhead because they are implemented under power stripes where are usually placed filler cells. This is an important result because in this example are placed 21335 SPS cells.

It is clear that presented design methodology provides designs with reduced maximal operational frequency. Power consumption and required silicon area are also degraded. On the other hand, the protection against latchup effect, as well as protection against single event upsets and transients require trade-off between required hardware, power consumption, maximal operating frequency and sufficient protection level against radiation effects.

In the following figure is presented a view of MW switch chip floor-plan, prepared using the developed fault-tolerant design methodology. In order to provide better routing, the PNC is placed around processor core as it is possible to notice in Fig. 9.

Placed SPS cell is presented in Fig. 10. It is important to note that stripes in MW switch processor core are generated using Metal3 layer. This is done because of control signals which are routed in Metal2 layer.

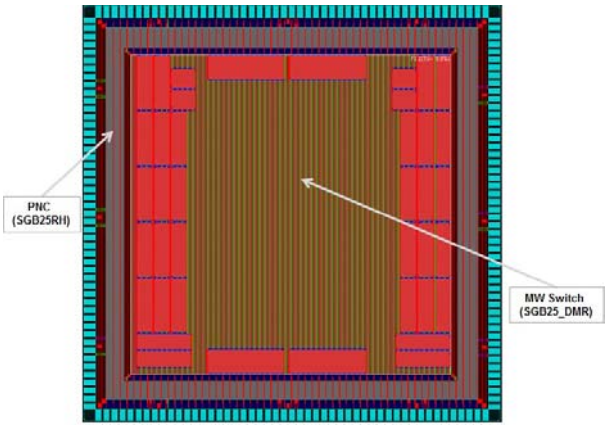

Fig. 9. Floor plan view of fault tolerant MW processor

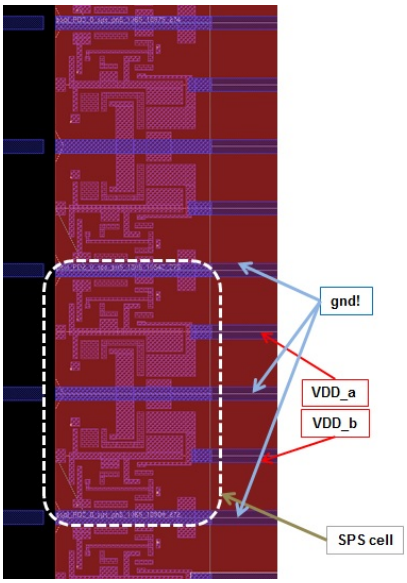

Fig 10. SPS cell placed and routed (special route only)

V. CONCLUSION

Advanced redundant circuits need a latchup protection in order to operate in a reliable manner. Therefore, this paper introduces and describes newly developed single event latchup (SEL) protection switches and a technique for their integration into an ASIC design.

The main contribution of the presented work is the introduction and development of a methodology for highly reliable digital ASIC designs based on redundant circuits with latchup protection. Based on the implementation figures, it is easy to notice that the proposed design methodology comes at the price of an overhead of area and power. It is important to note that the area and power overheads have two different causes. The first cause is the additional control logic used to support the power protection technique in redundant circuits. The second cause for the area and power overhead is the implementation of the power network controller (PNC), important for proper operation of all integrated SPS cells.

The SPS cell itself does not affect the area overhead due to the mechanism by which it is integrated into an ASIC. This was achieved by an innovative technique to utilize area normally reserved for filler cells, while staying in the standard design flow.

ACKNOWLEDGEMENT

The research leading to these results has received funding from the European Union's Seventh Framework Program FP7 (2007 - 2013) under the grant agreement no. 284389 also referred as VHiSSI.

REFERENCES

[1] J. Von Neumann, "Probabilistic Logics", Automata Studies, Princeton University Press, 1956

[2] R. E. Lyons, W. Vanderkulk, "The Use of Triple-Modular Redundancy to Improve Computer Reliability", IBM Journal April 1962

[3] M. P. Baze, S. P. Buchner, D. McMorrow, "A Digital CMOS Design Technique for SEU Hardening", IEEE Transaction on Nuclear Science, Vol. 47, No. 6, pp. 2603-2608, December 2000

[4] N. Rollins, M. Wirthlin, P. Graham, M. Caffrey, "Evaluating TMR Techniques in the Presence of Single Event Upsets", Military and Aerospace Programmable Logic Devices International Conference, Washington DC, USA, 2003

[5] J. Teifel, "Self-Voting Dual-Modular-Redundancy Circuits for Single-Event-Transient Mitigation", IEEE Transactions on Nuclear Science, VOL. 55, NO. 6, (pp. 3435-3439), December 2008

[6] D.B. Estreich, A. Ochoa, and R.W. Dutton, "An Analysis of Latchup Prevention in CMOS IC's Using Epitaxial Buried Layer Process", International Electron Device Meeting, 1978, pp. 76-84

[7] R.R. Troutman, "Epitaxial Layer Enhancement of n-Well Guard Rings for CMOS Circuits", IEEE Electron Devices, 1983, (pp. 438-440).

[8] S. Montenegro, V. Petrovic, and G. Schoof, "Network Centric Systems for Space Application," Advances in Satellite and Space Communications, SPACOM 2010, Page(s): 146 – 150

[9] V. Petrovic, M. Ilic, G. Schoof, and S. Montenegro, "Implementation of Middleware Switch ASIC Processor", IEEE Telfor Journal, Vol. 4, No. 2, 2012

[10] Maxwell Technologies, "Latchup Protection Technology™ (LPT) Overview", Available: http://www.maxwell.com/products/microelectronics/latchup-protection

[11] V. Petrovic, M. Ilic, G. Schoof, Z. Stamenkovic, "Design Methodology for Fault Tolerant ASICs", Proc. of the 15th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems Symposium (DDECS 2012), 8 (2012)

[12] Cadence Custom IC Design – Circuit Design, Available: http://www.cadence.com/products/cic/Pages/default.aspx

[13] IHP GmbH, Leibniz Institute Frankfurt Oder, Available: www.ihp-microelectronics.com